

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Thomas, et al.

Docket No.:

2003 P 54322 US

Serial No.:

10/790,907

Art Unit:

2811

Filed:

March 2, 2004

Examiner:

TBD

For:

Integrated Circuit with Re-Route Layer and Stacked Die Assembly

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Date of Deposit:

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Certificate of Mailing via First Class Mail (1 page) Information Disclosure Statement (1 page) PTO/SB/08A & 08B with 17 References Cited (2 pages) Copy of 1 Reference Cited Return Postcard

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits. In the event a fee is required, please charge any additional amount, or credit any overpayment to Deposit Acct. No.50-1065 of the below mentioned firm.

Pursuant to 37 CFR 1.98(a)(2)(i), as amended, copies of U.S. Patents cited are not being submitted. However, Applicant has included copies of any non-patent literature.

Respectfully submitted,

June 15, 2004

Date

Ira S. Matsil

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PTO/SB/08a (08-03)

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Complete if Known Substitute for form 1449A/PTO 10/790.907 Application Number INFORMATION DISCLOSURE Filing Date March 2, 2004 STATEMENT BY APPLICANT First Named Inventor Thomas, et al. Art Unit 2811 (Use as many sheets as necessary) **Examiner Name TBD** Sheet 1 2 of Attorney Docket Number 2003 P 54322 US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.1	Document Number Number - Kind Code ^{2 (# known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US-6,291,881 B1	09-18-2001	Yang	
	2	US-6,495,442 B1	12-17-2002	Lin, et al.	
·	3	US-6,514,794 B2	02-04-2003	Haba, et al.	
	4	US-6,555,917 B1	04-29-2003	Heo	
	5	US-6,560,117 B2	05-06-2003	Moon	
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	7	US-6,582,992 B2	06-24-2003	Poo, et al.	
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	15	US-2003/0160312 A1	08-28-2003	Lo, et al.	
	16	US-2003/0203537 A1	10-30-2003	Koopmans	
		US-			

	FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No.1	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²		
**************************************	17	KIM, G., "Pad-On-Circuit (PoC) Process and Its Application," 10th Annual International KGD Packaging & Test Workshop, Napa, CA (September 8-10, 2003) 27 pages.			
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